



MICHAEL ANDERSON

LEAD FPGA ENGINEER

CONTACT

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- San Francisco, CA

SKILLS

- FPGA Design
- VHDL
- SystemVerilog
- High-Frequency Trading
- ModelSim
- Project Management

LANGUAGES

- English
- Spanish
- French

EDUCATION

BACHELOR OF SCIENCE IN COMPUTER ENGINEERING, TECH UNIVERSITY, 2012

ACHIEVEMENTS

- Recognized for outstanding performance with the 'Excellence in Engineering' award in 2020.
- Developed a patented FPGA design that reduced latency in trading systems by 30%.
- Successfully led a project that resulted in a 15% cost reduction through optimized design processes.

PROFILE

With a decade of experience in FPGA design, I have developed a robust skill set that encompasses system architecture, design validation, and project management. My career has primarily focused on high-frequency trading applications, where I designed low-latency FPGA solutions that significantly enhanced transaction speeds. I have a unique blend of technical and managerial skills, allowing me to lead teams effectively while maintaining a hands-on approach to design.

EXPERIENCE

LEAD FPGA ENGINEER

Financial Tech Solutions

2016 - Present

- Led a team of engineers in designing FPGA solutions for high-frequency trading applications, achieving a 50% improvement in transaction speed.
- Conducted system architecture reviews to ensure compliance with regulatory standards.
- Utilized simulation tools to validate design functionality, leading to a 98% success rate in pre-production testing.
- Collaborated with software developers to integrate FPGA designs with trading algorithms.
- Trained new team members on design methodologies and tools, enhancing team productivity.
- Managed project timelines and deliverables, ensuring on-time completion within budget.

FPGA DESIGN ENGINEER

Quantum Tech Corp.

2014 - 2016

- Designed and implemented FPGA-based solutions for real-time data processing, improving throughput by 40%.
- Performed comprehensive testing and validation of FPGA designs, achieving significant reduction in post-deployment issues.
- Engaged in cross-functional collaboration to optimize system performance and minimize latency.
- Developed design documentation and user manuals for internal and client use.
- Participated in design reviews, providing insights that led to improved design efficiency.
- Contributed to the development of proprietary tools for FPGA design simulation.